

A STUDY OF POWER MINIMIZATION USING STRATEGY IN MOS TRANSISTOR USING QUASI-FLOATING-GATE

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The current trend for today's computing products has been mobile technology solutions. These products include cellular phones, laptop computers, personal digital assistants (PDA), and more. In order to provide reliable computing and communication devices such as the ones listed above, the components necessary to construct these devices must be designed for a low-power environment. This implies that the supply voltage and supply currents must be lowered to realize longer battery life and thus consumer approval. A novel design technique for closed-loop amplifier circuits, suited to very low supply voltages, is proposed. This paper will show a method known as Quasi-Floating-Gate (QFG) MOS transistors that allows the operation of amplifier circuits at very low supply voltages. QFG transistors are particularly suitable to applications involving closed-loop amplifier circuits based on multiple-input capacitive dividers. QFG transistors have noticeable gains over current floating gate MOS transistors in that floating-gate MOS structures are subject to Gain- Bandwidth product degradation and large initial floating gate charge. The applications presented in this paper are vital for the mobile system environment. Included herein are a programmable gain inverting amplifier, a sample and hold circuit, and a digital-to-analog converter, which are all composed of QFG input pair transistors. Each circuit will be discussed in detail as well as the building blocks for these circuits, including the QFG transistor.

