

ENERGY EFFICIENT VOLTAGE LEVEL SHIFTER USING 180nm CMOS TECHNOLOGY

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Level Shifters are widely used as output drivers for interfacing logic and functional devices or circuits. Level Shifter have the voltage conversion range from deep sub- threshold region to super threshold region. There are two types of Conventional Level Shifter namely, Cross Coupled Level Shifter and Current Mirror Level Shifter. The Cross coupled level shifter creates the strong contention between pull up and pull down network and it causes the functional failure when converting from deep sub threshold to super threshold region and also it leads to high static power and large area, slow conversion speed. To avoid this contention, current mirror structure is used instead of cross coupled one. One popular current mirror level shifter circuit is Wilson current mirror level shifter (WCLMS) that achieves the lower standby power but it suffers from large delay and area penalty. In this paper, pass transistor is used in such a way to increase the voltage swing at the input of output buffer. This in turn drastically reduces the static current flow through the first stage inverter of the output buffer. Also the circuit is modified such that the fall transition time at the input of output buffer is reduced. This is achieved by increasing the static current passing through the input node of the output buffer. In this way, the drawbacks of existing work on WCLMS are eliminated. To check the functionality, the proposed design is implemented in 180nm cadence and the results shows comparatively increased voltage swing and improved fall transition time. By utilizing the reduced swing buffer design for preventing the high static current, the proposed level shifter significantly reduces the standby power compared to WCMLS.